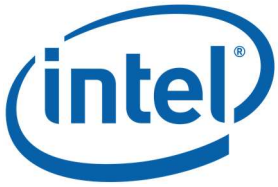

Kaby Lake Memory Reference Code Version 3.7.6

Release Notes

September 2019

Revision 3.7.6

Intel Restricted Secret

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1 Introduction

- Product: Kaby Lake Memory Reference Code
- Developed by: Intel Corporation
- Software version released date: <September/2019>

Note: This document is cumulative and includes information on previous versions. The version information is presented with the newest release first and then regressing through earlier versions.

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Note: This sample code is to be used in accordance with the DCL document that came with the samples. Refer to the DCL for intended purpose of the sample and recommendations for testing that should not be performed with these samples.

Note: **Visual Studio 2013 Update 5 patch is needed**.
Update with release information can be obtained at following link:
https://support.microsoft.com/en-in/help/3021976/description-of-visual-studio-2013-update-5

1.1 Purpose of Memory Reference Code (MRC)

This is sample reference code for memory detection and initialization of Kaby Lake Memory Reference Code. It supports detection and initialization of memory modules and complies with the requirements in the BIOS specification.

The Memory Reference Code is intended for use as part of Intel BIOS. An OEM may need to modify the code to meet specific platform designs, error handling features, platform specific BIOS features, or other local requirements.

1.2 Target Customers

The MRC code is intended for use as part of Intel BIOS. The code is compatible with both mobile and desktop products.

1.3 Related Documents

- Framework Client Bios 2016 Memory Reference Code help file (RC.chm)

- Framework Client Bios 2016 Memory Reference Code Porting Guide

1.4 Version Release History

Version	Description	Release Date
3.7.6	Updates to all other Kabylake platforms and supported OS.	Sep 04, 2019
3.7.5	Updates to all other Kabylake platforms and supported OS.	June 10, 2019
3.7.4	Aligning with GC for AML Y42/Y22 PV, Best Known Configuration (BKC) Software Package (Microsoft Windows* 10 - 64 bit 19H1) WW23'2019	June 4, 2019
3.7.3	Aligning with AML Y42/Y22 QS, Best Known Configuration (BKC) Software Package (Microsoft Windows* 10 -64 bit 19H1) WW18'2019	May 6, 2019
3.7.2	Aligning with Coffee Lake S82/62/42 Kaby Lake PCH-H Consumer Beta Best Known Configuration (BKC) Software Package (Microsoft Windows* 10 -64 bit 19H1) WW17'2019	April 24, 2019
3.7.1	Update for KBL-YR/KBL-R/KBL/CFL/AML	March 29, 2019
3.6.9	Aligning with AML Y42 RS5 Beta Best Known Configuration (BKC) (Microsoft Windows* 10 64-bit Redstone 5) WW03'2019	Jan 11, 2019
3.6.8	Aligning with CFL-S82/62/42-KBP-H-RS5 Consumer PV Best Known Configuration (BKC) RS5 WW51'2018	Dec 24, 2018
3.6.7.1	Aligning with KBL-U42 RS5 PV BKC WW51'2018	Dec 14, 2018
3.6.7	Update for KBL-YR/KBL-R/KBL/CFL/AML	Nov 16, 2018
3.6.6	Update for KBL-YR/KBL-R/KBL/CFL/AML	Nov 15, 2018
3.6.5	Aligning with Coffee Lake S82/62 , Kaby Lake PCH-H Beta Best Known Configuration (BKC) (Microsoft Windows* 10 64-bit Redstone 5) WW43'2018	October 22, 2018
3.6.4	Aligning with AML Y22 5W RS5 Beta WW40'2018	September 28, 2018
3.6.3	Aligning with Coffee Lake S82, Kaby lake PCH-H PV Best Known Configuration (BKC) (Microsoft Windows* 10 64-bit Redstone 4) WW37'2018	September 11, 2018
3.6.2	No update – Align with AML-Y22 7W PV BKC WW31 '2018	August 3, 2018
3.6.1.1	No update – Align with KBL-R RS4 PV BKC WW32 '2018	August 3, 2018
3.6.1	Aligning with AML-Y22 5W PR1 BKC WW29'2018	July 20, 2018
3.6.0	Aligning with KBL-G RS4 Corp BKC release WW26'2018	June 29, 2018
3.5.0	Aligning with Coffee Lake S82, KBP-H Beta Best Known Configuration (BKC) (Microsoft Windows* 10 64-bit RS3) WW25	June 20, 2018
3.4.0	Update for KBL-R/KBL/CFL	June 20, 2018

3.3.0	Update for KBL-R/KBL/CFL	May 21, 2018
3.2.1	Update for KBL-R/ KBL/ CFL	May, 2018
3.2.0	**KBL/KBL-R/KBL-YR** Aligning with KBL-YR RS4 BKC WW15	April, 2018
3.1.0	**CFL-S with Kaby Point PCH** Aligning with CFL-S62/S42 + KBP-H Consumer PV BKC WW03 RS3	Jan 16 , 2018
3.0.1	**KBL/KBL-R PR1** Aligning with KBL-Y22 PV, KBL U22 PV, KBL U23e PV and KBL R PR1 BKC	Dec 21, 2017
3.0.0	**KBL/PV** **KBL-R/ PV** Aligning with KBL legacy U22/S42/H42 PV BKC release WW49	Dec 6, 2017
2.9.2	CFL-S with Kaby Point PCH Aligning with CFL-S62/S42 + KBP-H BKC WW47 RS3	Nov 22, 2017
2.9.0	KBL/KBL-R RS3 WW44 BKC Aligning with KBL/KBL-R WW44 BKC RS3	Nov 1, 2017
2.8.1	KBL/KBL-R RS3 WW41 BKC Aligning with KBL/KBL-R BKC WW41 RS3	Oct 11, 2017
2.8.0	KBL/KBL-R RS3 WW39 BKC RS3 Aligning with KBL/KBL-R BKC WW39 RS3	Sep 29, 2017
2.7.2	KBL/KBL-R RS3 WW36 BKC RS3 CFL-S with Kaby Point PCH PR1 RS2 Aligning with KBL/KBL-R BKC WW36 RS3 & CFL S 62 /CFL S 42 + KBP-H PCH PR1 RS2	Sep 7, 2017
2.7.0	KBL/KBL-R RS3 WW33 BKC CFL-S with Kaby Point PCH Aligning with KBL/KBL-R BKC release WW33 RS3	Aug 17, 2017
2.6.2	KBL/PV KBL-R/PV CFL-S with Kaby Point PCH Consumer PV RS2 Aligning with CFL-S + KBP-H PCH Consumer PV BKC release WW32 RS2	Aug 8, 2017
2.6.1	KBL/PV KBL-R/PV CFL-S with Kaby Point PCH Beta Aligning with CFL-S with Kaby Point PCH WW31 BKC release	Aug 2, 2017
2.6.0	KBL/PV KBL-R/PV CFL-S with Kaby Point PCH Beta Aligning with CFL-S with Kaby Point PCH BKC release	July 18, 2017

2.5.1	KBL/PV KBL-R/ PV CFL-S with Kaby Point PCH Beta Aligning with KBL/KBL-R RS2 corporate PV BKC Release.	July 4, 2017
2.5.0	Update for All KBL platform	June 22, 2017
2.4.0	KBL-R PC/PV RS2 PC/PV CFL-S with Kaby Point PCH Beta	June 1, 2017
2.3.0	Updates to Coffee lake with PCH Z370 platform support	May 17, 2017
2.2.0	KBL-R Beta Post SR'17 update	April 25, 2017
2.1.0	KBL-R Beta Post SR'17 update	April 7, 2017
2.0.0	KBL-R Beta Post SR'17 update	March 22, 2017
1.9.0	KBL-R Beta Post SR'17 update	March 09, 2017
1.8.0	KBL-R Beta Post SR'17 update	February 14, 2017
1.7.0	KBL-R Beta Post SR'17 update	February 06, 2017
1.6.0	Post SR'17 update for PR2	January, 2017
1.5.0	PV SR'17 H – consumer PC/PV* SR'17 S42/H/ and Y/U22 – Corporate* Beta SR'17 S22 with RS1	December 2, 2016
1.4.1	PV for SKL CPU on KBL boards with win 7/8.1 First Post SR'17 PV update BKC release (U32e and S22)	November 18, 2016
1.4.0	Update for all Kabylake platforms	November 4, 2016
1.3.0	PV SKL on KBL Platforms with Win7/Win8.1 Post SR'17 update – PR2 Update to U23e	Octorber, 2016
1.2.0	PV U/Y HR'16 RS1 Update SR'17 S/H/Y/U Update U23e RS1	Octorber, 2016
1.1.0	PV SR'17 S42 – consumer PCV SR'17 Y/U Update PCV SR'17 H/U32e/ all Corp SKUs	September, 2016
1.0.5	Update for all Kabylake platforms.	Augst 25, 2016
1.0.4	Update for PR3 Update for HR'16 RS1 Update for SR'17 S/H/Y/U/U23e	Augst 11, 2016
1.0.3	Update for HR'16 Update for SR'17 S/H/Y/U/U23e	July 21, 2016

1.0.2	No Update for MRC	July 1, 2016
1.0.1	U/Y PV Update, DT with SPT Alpha Update	June 16, 2016
1.0.0	• U/Y Production candidate • DT with SPT Alpha Cons/Corp update • Halo Alpha Cons/Corp update	June 7, 2016
0.9.1	• U/Y Production candidate • DT with SPT Alpha Cons/Corp update • Halo Alpha Cons/Corp update	June 2, 2016
0.9.0	• U/Y PC candidate • DT with SPT Alpha Cons/Corp update • Halo Alpha Cons/Corp update	May 17, 2016
0.8.1	U/Y Beta Update	May 09, 2016
0.8.0	U/Y Beta Update and QS support Update to Desktop Alpha Update to H	April 19, 2016
0.7.3	U/Y Beta Update DT with SPT Alpha Cons/Corp Halo Alpha Cons/Corp	April 6, 2016
0.7.2	Mobile Beta update	March 16, 2016
0.7.1	Kaby Lake U/Y Beta release update	March 8, 2016
0.7.0	Kaby Lake U/Y Beta release	Febuary 23, 2016
0.6.1	Kaby Lake Alpha release	January 28, 2016
0.6.0	Kaby Lake U/Y Alpha release	January 7, 2016
0.5.0	Initial external release	December 3, 2015

2 Version 3.7.6 Details

2.1 New Features

N/A

2.2 Fixed Bugs

N/A

3 Version 3.7.5 Details

3.1 New Features

N/A

3.2 Fixed Bugs

N/A

4 Version 3.7.4 Details

4.1 New Features

N/A

4.2 Fixed Bugs

N/A

5 Version 3.7.3 Details

5.1 New Features

N/A

5.2 Fixed Bugs

5.2.1 Bug Name 1

- Description

  Fixed CPU stepping showing unknown in BIOS page for CFL-S-KBPH R0 config

- Solution

  Add support for CFL-S R0 stepping

- Platform Affected

  CFL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

6 Version 3.7.2 Details

6.1 New Features

6.1.1 Feature 1

- Description / Solution

  Add 64-bit PCI MMIO Read/Write support

- Platform Affected

  KBL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/PeiDxeSmmMemoryAddressEncodeDecodeLib/MemoryAddressEncodeDecodeLib.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

6.1.2 Feature 2

- Description / Solution

  Remove High-Z from DDR4 RttWr values due to EV recommendation

- Platform Affected

  KBL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

6.2 Fixed Bugs

6.2.1 Bug Name 1

- Description

  Fix failure during Round Trip Latency training with LPDDR3 memory, with certain bytes reporting failing margin response

- Solution

  New flow is changing CLK while CKE is OFF, which makes it robust

- Platform Affected

  AML, KBL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

6.2.2 Bug Name 2

- Description

  Refresh 2X Status does not indicate when the MC is in 2X Refresh

- Solution

  Code update whene CLTM_ENABLE is set

- Platform Affected

  AML, KBL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/Include/ConfigBlock/MemoryConfig.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcPowerModes.c

7 Version 3.7.1 Details

7.1 New Features

7.1.1 Feature 1

- Description / Solution

  Add MRC Related Board Support for AML-Y 42 CC Board

- Platform Affected

  KBL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

7.2 Fixed Bugs

N/A

8 Version 3.6.9 Details

8.1 New Features

N/A

8.2 Fixed Bugs

N/A

9 Version 3.6.8 Details

9.1 New Features

9.1.1 Feature 1

- Description / Solution

  Update DDR4 WrV Conversion Calculation for Retrain Margin Limits, this calculation would implement a better rounding mechanism so that the Retrain Margin Limit check is properly applied to MRC

- Platform Affected

  KBL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

9.2 Fixed Bugs

9.2.1 Bug Name 1

- Description

  With certain populations of 2DPC DDR4, training failures can occur during "Write Voltage Centering" training step

- Solution

  For DDR4 WrV, instead of using ChangeMargin, directly call UpdateVrefWaitTilStable which will set WrV for the specific Channel/Rank, instead of using Multicast for either Rank/Channel

- Platform Affected

  KBL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

10 Version 3.6.7.1 Details

10.1 New Features

N/A

10.2 Fixed Bugs

N/A

11 Version 3.6.7 Details

11.1 New Features

11.1.1 Feature 1

- Description / Solution

  Add new CPUID Steppings support for AML W0/V0

- Platform Affected

  AML platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Common/CpuRegs.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

11.2 Fixed Bugs

N/A

12 Version 3.6.6 Details

12.1 New Features

N/A

12.2 Fixed Bugs

N/A

13 Version 3.6.5 Details

13.1 New Features

N/A

13.2 Fixed Bugs

N/A

14 Version 3.6.4 Details

14.1 New Features

14.1.1 Feature 1

- Description / Solution

  Enable CMDDSEQ step for KBL LP3 2133 to improve CMD timing margin

- Platform Affected

  KBL platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

14.2 Fixed Bugs

14.2.1 Bug Name 1

- Description

  A number of warning messages seen during DqTimeCentering1D training steps with certain ranks reporting clamping when setting TxVref (WrV)

- Solution

  For Ddr4 WrV cases within DqTimeCentering1D make sure that the ChangeMargin calls do not have the EnMultiCast bit set, avoiding possible WrV Clamping warning messasges.

- Platform Affected

  All platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

15 Version 3.6.3 Details

15.1 New Features

15.1.1 Feature 1

- Description / Solution

  Merge updated MRC changes:

  - Dimm odt training slot1 odt park calibration based on training of slot1 (was based on slot0 training)
  - Dimm odt training optimization function changed in margin training mode to be more rd/wr balanced based on UPM limits
  - RoundTripLatency step fix keeps IOLatency register value from under/overflow. In this case initial latency values are restored. Without this fix TAT step failed in long flyby topology.
  - TurnAroundLatency step fix adding guardband to DQS PI so it would stay greater then 64ticks while sweeping for margins

- Platform Affected

  All platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCommon.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCrosser.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/ReadTraining/MrcReadReceiveEnable.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

15.1.2 Feature 2

- Description / Solution

  Add extended memory ratios support for MRC Fastboot

- Platform Affected

  All platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcSaveRestore.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

15.2 Fixed Bugs

15.2.1 Bug Name 1

- Description

  Fix initial DRAM temperature programming per-rank

- Solution

  DDR4/LPDDR3 rank temperature register has to be programmed to "Hot" temperature befure the first LPDDR3/DDR4 temperature read occurs.

- Platform Affected

  All platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Restricted/MrcVersionTemplate.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcReset.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcReset.c

15.2.2 Bug Name 2

- Description

  Fix teamcity build errors

- Solution

  Necessary changes to fix duplicated naming for supporting VS2015 compiler.

- Platform Affected

  All platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcInterpreter.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.h

15.2.3 Bug Name 3

- Description

  BDAT pointer is zeroed out when MRC executes Retraining due to failure in retrain margin check

- Solution

  MRC should save/restore this pointer information prior to zeroing out the Outputs structure when executing Retraining path.

- Platform Affected

  All platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcBdat.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

15.2.4 Bug Name 4

- Description

  Build error after enabling PcdSsaFlagEnable and PcdEvLoaderEnable

- Solution

  Remove duplicate structure definition.

- Platform Affected

  AML platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcRmtData.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/SsaResultsConfig.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

16 Version 3.6.2 Details

16.1 New Features

N/A

16.2 Fixed Bugs

N/A

17 Version 3.6.1.1 Details

17.1 New Features

N/A

17.2 Fixed Bugs

N/A

18 Version 3.6.1 Details

18.1 New Features

18.1.1 Feature 1

- Description / Solution

  Merge Overclocking Changes:

  - NMode should not default to N:1 mode when used with XMP Profile, User should be able to select NMode regardless of which SPD Profile
  - Add missing frequencies to DdrFreqLimit in BIOS setup option
  - When calculating tCK For XMP profiles, when User profile is selected, the tCK value will not be limited by MemoryClockMax. This will allow the displayed XMP timings to be accurate based on XMP SPD, not artificially limited by OC Enable/Disable.

- Platform Affected

  KBL, CFL and AML platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

18.2 Fixed Bugs

18.2.1 Bug Name 1

- Description

  MRC senses a failure in SenseAmp Offset Training but doesn't assert when a bit fails to flip

- Solution

  Add conditional check if there are any bits which fail to flip during the initial Vref stage in SenseAmpOffset Training

- Platform Affected

  KBL, CFL and AML platforms

- Affected Files:

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

19 Version 3.6.0 Details

19.1 New Features

N/A

19.2 Fixed Bugs

N/A

20 Version 3.5.0 Details

20.1 New Features

N/A

20.2 Fixed Bugs

N/A

21 Version 3.4.0 Details

21.1 New Features

21.1.1 Feature 1

- Description / Solution

  Expose DDR4 memory timings for Memory Custom profile.

- Platform Affected

  CFL and KBL platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcSaveRestore.c

21.2 Fixed Bugs

21.2.1 Bug Name 1

- Description

  Frequency limitation should be applied to 2DPC U-DIMM Configurations with Mixed Part Numbers

- Solution

  During SPD Processing, if MRC detects a 2DPC Mixed U-DIMM configuration and the frequency is set to 2667, then MRC will reduce the frequency requested to 2400

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcSpdData.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/PeiMemoryInitLib.inf

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/PeiMemoryInitLibFsp.inf

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcDebugPrint.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcSaveRestore.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

21.2.2 Bug Name 2

- Description

  System may get failures with Hynix C die memory

- Solution

  Limit MRC values for CMDEQ, CMDDS and CMDSR training

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

21.2.3 Bug Name 3

- Description

  Fix SA Klocwork issue

- Solution

  Make sure dereferencing of MemorySchema pointer is possible only if MrcGetHobForDataStorage was successful

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcBdat.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

22 Version 3.3.0 Details

22.1 New Features

22.1.1 Feature 1

- Description / Solution

  Updated code base for new changes:

  1. Add Setup option to skip Software MemTest on Warm Boot

  2. Bug fix for error message in 2D Centering steps, when one bytes fails the entire margin parameter sweep.

  3. Only applying Turnaround Time increase for Rd2Rd_SG and Rd2Rd_DG if LPDDR3 is not used.

  4. Add Setup option for Enable/Disable BER within RMT.

- Platform Affected

  CFL and KBL platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/Include/ConfigBlock/MemoryConfig.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

22.2 Fixed Bugs

22.2.1 Bug Name 1

- Description

  Fix Teamcity Errors

- Solution

  Code update

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcBdat.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

22.2.2 Bug Name 2

- Description

  Merge CFL MRC changes to KBL MRC for below issues:

  1. Fixed memory margin issue with DDR4 2667 UDIMM
  2. Implement improvements from EV feedback

- Solution

  Code update

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCommon.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcDdr3.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

23 Version 3.2.1 Details

23.1 New Features

N/A

23.2 Fixed Bugs

N/A

24 Version 3.2.0 Details

24.1 New Features

N/A

24.2 Fixed Bugs

N/A

25 Version 3.1.0 Details

25.1 New Features

N/A

25.2 Fixed Bugs

N/A

26 Version 3.0.1 Details

26.1 New Features

N/A

26.2 Fixed Bugs

N/A

27 Version 3.0.0 Details

27.1 New Features

N/A

27.2 Fixed Bugs

N/A

28 Version 2.9.2 Details

28.1 New Features

N/A

28.2 Fixed Bugs

28.2.1 Bug Name 1

- Description

  Failures seen during Late Command Training on 32GB system, with strange out of CLK PI bounds behavior

- Solution

  1. Check PI Setting bounds when determining the CLK Sweep range at the beginning of LCT.

  2. Adjust logic for WrapAllowed in CmdLinearFindEdges so that it will only be allowed if the lower PI setting is 0.

  3. Add additional checks for "Ddr4DdpSharedClock" in new code which also shifts CLK signals per-rank.

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

28.2.2 Bug Name 2

- Description

  PDA Operation is failing due to DQ Offset settings

- Solution

  Update PDA Enter/Exit flow

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

28.2.3 Bug Name 3

- Description

  System is hanging at Postcode dd80 with CATERROR

- Solution

  Add logic to check the bounds of CMD/CTL/CLK signals separately from the checks for DqPis

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

29 Version 2.9.0 Details

29.1 New Features

N/A

29.2 Fixed Bugs

29.2.1 Bug Name 1

- Description

  Random BSOD found with Micron LPDDR3 2133MHz 16GB Memory, when system is trained at cold temperature, and memory tested at high temperature

- Solution

  Add guardband in RoundTrip latency to account for possible tDQSCK drift

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/ReadTraining/MrcReadReceiveEnable.c

30 Version 2.8.1 Details

30.1 New Features

N/A

30.2 Fixed Bugs

N/A

31 Version 2.8.0 Details

31.1 New Features

31.1.1 Feature 1

- Description / Solution

  Expose all memory timings for Memory Custom profile, adding the setting of Turnaround Timing registers within override structure

- Platform Affected

  CFL and KBL platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

31.2 Fixed Bugs

N/A

32 Version 2.7.2 Details

32.1 New Features

32.1.1 Feature 1

- Description / Solution

  Expose all memory timings for Memory Custom profile, Adding Turnaround Timings to BIOS Setup Menu for Overclocking Memory Timings

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

32.2 Fixed Bugs

32.2.1 Bug Name 1

- Description

  With SAGV Enabled, tREFI should be reduced to prevent DRAM corruption. And fixed DDR4 User Profile limits for tCL Mask in SPD Processing

- Solution

  Subtract 2.8% from jedec tREFI when SAGV enabled to make up for any refresh deficit

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcRefreshConfiguration.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

32.2.2 Bug Name 2

- Description

  MRC is not detecting memory topology changes correctly

- Solution

  Swtich MRC to the default profile, when memory topology changes

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcSaveRestore.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

33 Version 2.7.0 Details

33.1 New Features

33.1.1 Feature 1

- Description / Solution

  Update SMBIOS Memory Info Data HOB Structure name and parameters for generic accross platforms

- Platform Affected

  Kaby Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

33.2 Fixed Bugs

33.2.1 Bug Name 1

- Description

  ChannelClkPiCode array can possibly be used with uninitialized array elements

- Solution

  Use MrcSetMem to initialize the array to zero

- Platform Affected

  Kaby Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

34 Version 2.6.2 Details

34.1 New Features

34.1.1 Feature 1

- Description / Solution

  Add voltage control for Vccio, VccSA, VccSFR_OC and VccST

- Platform Affected

  Kaby Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/Library/PeiSaPolicyLib/MrcOemPlatform.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcDdr3.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

34.2 Fixed Bugs

N/A

35 Version 2.6.1 Details

35.1 New Features

35.1.1 Feature 1

- Description / Solution

  Add CPU stepping for CFL-S 4 +2

- Platform Affected

  Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

35.2 Fixed Bugs

35.2.1 Bug Name 1

- Description

  Late Command Training corner case failure seen with certain memory configurations

- Solution

  This error check is now erroneous and should be removed

- Platform Affected

  Coffee Lake

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

35.2.2 Bug Name 2

- Description

  tRRD value is being set outside of boundary for SaSetup. However DDR4 doesn't use tRRD timing, instead it uses tRRD_S and tRRD_L

- Solution

  Set tRRD to 0 for DDR4

- Platform Affected

  Kabyc Lake

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

36 Version 2.6.0 Details

36.1 New Features

36.1.1 Feature 1

- Description / Solution

  Add CPUID values for CFL 8 +2 P0

- Platform Affected

  Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Common/CpuRegs.h

36.1.2 Feature 2

- Description / Solution

  Increase Max Memory Ratio for Overclocking with CFL stepping CPUs

- Platform Affected

  Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcTypes.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcApi.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcRegisters/MrcMcRegister5xxx.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcRegisters/MrcMcRegisterStruct5xxx.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

36.1.3 Feature 3

- Description / Solution

  Implement long term solution for Xml CLI

- Platform Affected

  Kaby Lake and Coffee Lake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcMemoryMap.c

36.2 Fixed Bugs

36.2.1 Bug Name 1

- Description

  CFL-S CPU (QDF: Q7FT) with 2DPC 2667 DDR4 U-DIMM installed has limited maximum frequency to 2400MHz. 1DPC Configuration boots well at 2667 MHz

- Solution

  MRC should not modify DDR4 DMFC for CFL-S CPU (0x906EA)

- Platform Affected

  Coffee Lake

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

37 Version 2.5.1 Details

37.1 New Features

N/A

37.2 Fixed Bugs

37.2.1 Bug Name 1

- Description

  Fix error in calculation for ShiftPI in special case in Pi Reserves changes

- Solution

  Move all bus PIs within the WL Flyby step, to allow WL robbustness and margining range for further training steps

- Platform Affected

  KabyLake and Coffee Lake

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

38 Version 2.5.0 Details

38.1 New Features

38.1.1 Feature 1

- Description / Solution

  Updates for new requirements (long fly-by):

  1. Dq Pi Reserves Changes
  2. Adding Read Voltage Centering during MrcReadODTTraining
  3. Increasing Write and Read DIMM ODT Duration by 1 for DDR4 on H/S SKUs
  4. Update CMD Loop Count for RMT, from 10 to 17
  5. Update MrcGetBERMarginByte() to check RcvEnaX for MrcCalcMaxRxMargin

- Platform Affected

  None

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCommandTraining.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCommon.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

38.2 Fixed Bugs

N/A

39 Version 2.4.0 Details

39.1 New Features

N/A

39.2 Fixed Bugs

N/A

40 Version 2.3.0 Details

40.1 New Features

N/A

40.2 Fixed Bugs

40.2.1 Bug Name 1

- Description

  Workaround for display underrun in KBL 23e when pressing WIN key - two 4K panels and EDRAM SW always-on mode

- Solution

  Adjust Channel Hash Mask value for KBL 23e SKU

- Platform Affected

  KBL 23e SKU

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/Library/PeiSaPolicyLib/PeiSaPolicyLib.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Common/CpuRegs.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

40.2.2 Bug Name 2

- Description

  Improve DDR OC capability

- Solution

  To avoid hang during Round Trip Latency training at higher frequencies, Page Close Idle Timer should be extended prior to training

- Platform Affected

  KBL Platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/ReadTraining/MrcReadReceiveEnable.c

41 Version 2.2.0 Details

41.1 New Features

41.1.1 Feature 1

- Description / Solution

  Additional Changes for KBL-R LPDDR3 MiniBIOS enabling:

  Set DqPinsInterleaved to 0,

  Enable SPD_PRSNT jumper support

- Platform Affected

  None

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

41.2 Fixed Bugs

41.2.1 Bug Name 1

- Description

  Fix SA klocwork issues

- Solution

  Add check to skip Rank index if OtherRank is equal to MAX_RANK_IN_CHANNEL

- Platform Affected

  KBL platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

41.2.2 Bug Name 2

- Description

  Remove Read Dependency from Early Write Centering Training Steps

- Solution

  When shifting RD2RD_SG, RD2RD_DG should also be shifted by the same amount

- Platform Affected

  KBL platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.c

41.2.3 Bug Name 3

- Description

  Realign Capsule memory allocation not to conflict with Crashdump support

- Solution

  Move the capsule memory allocation after Crashdump adjustment happens

- Platform Affected

  KBL platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

42 Version 2.1.0 Details

42.1 New Features

42.1.1 Feature 1

- Description / Solution

  Add support for KBL-R LPDDR3 in miniBios

- Platform Affected

  KBL-R platforms

- Affected Files:

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Common/PlatformBoardId.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c#

/KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

42.1.2 Feature 2

- Description / Solution

  Enable LPDDR3 ODT Training for 2133+ Frequency

- Platform Affected

  KBL-R platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h#25 edit

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcSchedulerParameters.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcReset.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

42.2 Fixed Bugs

42.2.1 Bug Name 1

- Description

  Remove Read Dependency from Early Write Centering Training Steps

- Solution

  Apply increase to Read-to-read same group Turn Around Time before these Write training steps to avoid any unintentional read stress due to non-optimal Read center point. After the training step is complete, the original Turnaround Timing value is re-applied.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.c

42.2.2 Bug Name 2

- Description

  System will hang up by doing S4 long run with single 16G DDR4 DIMM populated

- Solution

  Based on DDR4 spec, there shoule be no termination when the rank is in self refresh.

- Platform Affected

  KBL-H platforms

- Affected Files:

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

43 Version 2.0.0 Details

43.1 New Features

- Description / Solution

  Include MemInfoHob in FspmUpd.h

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcSpdData.h

43.2 Fixed Bugs

43.2.1 Bug Name 1

- Description

  During Turn Around Trip Training where initial values for WR2RD and WR2WR for Different DIMM/Different Rank fail due to mismatched delays between ranks

- Solution

  TurnAround Timing Adjustment after JEDEC Write Leveling

- Platform Affected

  KBL platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcTypes.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

43.2.2 Bug Name 2

- Description

  GMADR Base was incorrectly masked off which caused HSTI test failed when 64 bit MMIO is used

- Solution

  Correct mask bitmap setting for GMADR in SecureMemoryMapConfiguration.c

- Platform Affected

  KBL platforms

- Affected Files:

/KabylakeSiliconPkg/Hsti/Dxe/SecureMemoryMapConfiguration.c

44 Version 1.9.0 Details

44.1 New Features

N/A

44.2 Fixed Bugs

N/A

45 Version 1.8.0 Details

45.1 New Features

45.1.1 Feature 1

- Description / Solution

  Add support for SH file format

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiEvLoaderLib/EvLoaderPeim.c

45.1.2 Feature 2

- Description / Solution

  Add support for KBL U Refresh

- Platform Affected

  KBL-R platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Common/PlatformBoardId.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

45.2 Fixed Bugs

45.2.1 Bug Name 1

- Description

  Clean up of #if 0 directives

- Solution

  Clean up "#if 0" code for external release

- Platform Affected

  KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcSsaServices.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Hal/MrcRegisterCache.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Hal/MrcRegisterCache.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

45.2.2 Bug Name 2

- Description

  DDR4 Rank Interleave I/O buffer switching mismatch between KBL-S memory controller and SK hynix 2400 ECC UDIMM 2Rx8

- Solution

  Turn Around Training step is failing at 2400. Need to increase the initial TAT values for RD2RD, WR2WR, and WR2RD for Different Dimm and Different Rank. This applies to any system with Raw Card E1 and B1 DDR4 UDIMMS at 2400+

- Platform Affected

  KBL-S platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

46 Version 1.7.0 Details

46.1 New Features

N/A

46.2 Fixed Bugs

N/A

47 Version 1.6.0 Details

47.1 New Features

47.1.1 Feature 1

- Description / Solution

  Set McdecsMisc.Bits.Spare_RW=0x13 to enable IPC feature validation

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcSchedulerParameters.c

47.1.2 Feature 2

- Description / Solution

  Update CPUID for KBL-R in MRC and MiniBIOS

- Platform Affected

  KabyLake R platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.hSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Common/CpuRegs.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

47.2 Fixed Bugs

47.2.1 Bug Name 1

- Description

  When the system enters into Deep S3, the RSMRST# signal is asserted causing the DISB to be cleared. Due to DISB cleared, when the system is next restarted MRC will not take Warm Reset path and causes system black screen

- Solution

  On S3 MRC path after registers are restored, MRC should set DISB so we don't have any issues on subsequent resets

- Platform Affected

  KabyLake mobile platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

47.2.2 Bug Name 2

- Description

  After tDQSCK training (RcvenX), MMR after was getting corrupted

- Solution

  To reset DDRIO after any MRC step where move RxDQ/Rcven to ensure DDRPHY is not corrupted

- Platform Affected

  KabyLake mobile platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/ReadTraining/MrcReadDqDqs.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

48 Version 1.5.0 Details

48.1 New Features

N/A

48.2 Fixed Bugs

N/A

49 Version 1.4.1 Details

49.1 New Features

N/A

49.2 Fixed Bugs

49.2.1 Bug Name 1

- Description/Solution:

  Memory configuration represented incorrectly under BIOS setup menu on Kaby Lake H platform (Memory manufacture name is incorrectly represented on BIOS setup menu)

- Platform Affected

  KabyLake H Platform

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

50 Version 1.4.0 Details

50.1 New Features

50.1.1 Feature 1

- Description / Solution

  Memory Address Decoder UEFI Driver accessible from the UEFI shell. Separated the Memory Address Encode/Decode Logic from MRC into Public Base Library. Added definition of Memory Address Encode Decode Protocol and publishing of Memory Address Encode Decode Protocol in SaInitDxe.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/Library/MemoryAddressEncodeDecodeLib.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/PeiDxeSmmMemoryAddressEncodeDecodeLib/MemoryAddressEncodeDecodeLib.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/PeiDxeSmmMemoryAddressEncodeDecodeLib/PeiDxeSmmMemoryAddressEncodeDecodeLib.inf

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/PeiMemoryInitLib.inf#

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/PeiMemoryInitLibFsp.inf

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/AddrDecode/MrcMcAddrDecode.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/AddrDecode/MrcMcAddrDecode.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/BUILD/MiniBios.mak

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MiniMrc.mak

50.1.2 Feature 2

- Description / Solution

  Add memory info for resource calculate. Add revision history and incremented the revision.

- Platform Affected

  All KabyLake platforms

- Affected Files:

/KabylakeFspBinPkg/Include/MemInfoHob.h

/KabylakeSiliconPkg/SystemAgent/Include/MemInfoHob.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

50.1.3 Feature 3

- Description / Solution

  Enable and Disable the iMMA control flag settings (EvLoader and EvLoaderdelay setting) over BIOS Setup menu option for KBL/SKL platform iMMA memory Training.

- Platform Affected

  All Skylake / KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiEvLoaderLib/EvLoaderPeim.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

50.1.4 Feature 4

- Description / Solution

  Add hook for checking memory initial fail.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/PeiMemoryInitLibFsp.inf

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

50.2 Fixed Bugs

50.2.1 Bug Name 1

- Description:

  Shifting a negative value is undefined in C languages, CLANG compiler throws error.

- Solution

  Correct code for fixing compiling failure

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

50.2.2 Bug Name 2

- Description:

  ECC Bit level results are not printed in DqTimeCentering1D.

- Solution

  Add ECC Bit debug prints making use of already existing register read

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

50.2.3 Bug Name 3

- Description:

  Link CmdTristateDis from BIOS Setup to Memory Configuration block.

- Solution

  CmdTristateDis needs to be linked to the MEMORY_CONFIGURATION block

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

50.2.4 Bug Name 4

- Description:

  BIOS hangs at postcode 0xDD23 when BCLK is set to 300MHz.

- Solution

Added MrcData structure to MrcGetCpuTime(), which retrieves the BclkFrequency from MrcInputs to use in Time base calculation

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcMemoryScrub.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Hal/MrcHalMiddleLevel.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcDdr3.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcIoControl.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcReset.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Ssa/BiosSsaCommonConfig.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.h

50.2.5 Bug Name 5

- Description:

  Command stretch with N:1 is not working.

- Solution

  MRC should tune command rate according to the BIOS setup option.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h#

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

50.2.6 Bug Name 6

- Description:

  Memory Voltage option inside the Overclocking menu to adjust VDD down from 1.2V to 1.10V.

- Solution

  Change default setting from 1.2V to 1.1V

- Platform Affected

  KabyLake-U based platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcMcConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

50.2.7 Bug Name 7

- Description:

  BIOS is not behaving as expected when mixing XMP and non-XMP DDR4 module.

- Solution

  Changed behavior when new DIMM is detected - If selected memory profile is XMP1 or XMP2, this will be overidden to be STD_PROFILE

  Removed Compare Memory Profiles and replaced with timing checks during SPD processing

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Restricted/Scripts/SpdParse.py

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

50.2.8 Bug Name 8

- Description:

  KW scan error fix.

- Solution

  Fix StartOffset array elments might be used uninitialized in MrcWriteLeveling.c

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

50.2.9 Bug Name 9

- Description:

  Capsule update scatter gather corruption.

- Solution

  Basically it rearranged the code in MRC so the memory descriptor hobs were published before validating the capsule. This allows the capsule code to check the scatter gather list against the real memory descriptors to make sure we don't dereference a bad address

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

50.2.10 Bug Name 10

- Description:

  Cat err (MCA error) seen when SA GV memory frequency set to 1200 MHz.

- Solution

  Put the modified OddRatioMode in MrcOutput structure, keeping the original MrcInput->OddRatioMode intact.

  Save OddRatioMode per SAGV point in MrcSave structure

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/Include/ConfigBlock/MemoryConfig.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcDebugPrint.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcSaveRestore.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

51 Version 1.3.0 Details

51.1 New Features

N/A

51.2 Fixed Bugs

N/A

52 Version 1.2.0 Details

52.1 New Features

N/A

52.2 Fixed Bugs

N/A

53 Version 1.1.0 Details

53.1 New Features

N/A

53.2 Fixed Bugs

N/A

Version 1.0.5 Details

53.3 New Features

N/A

53.4 Fixed Bugs

53.4.1 Bug Name 1

- Description:

  Cat err (MCA error) seen when SA GV memory frequency set to 1200 MHz.

  When OddRatioMode is automatically enabled during SAGV Low point, it's also applied to SAGV High point, which is incorrect..

- Solution

  Put the modified OddRatioMode in MrcOutput structure, keeping the original MrcInput->OddRatioMode intact. Save OddRatioMode per SAGV point in MrcSave structure. Additional changes:

  - Enable proper MRC logging in SAGV flow in LOCAL_STUB mode.

  - Add Setup help string to mention that FreqSaGvLow should be below or equal to SAGV High frequency.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakePlatSamplePkg/Setup/SaSetup.uni

  /KabylakeSiliconPkg/SystemAgent/Include/ConfigBlock/MemoryConfig.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcDebugPrint.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcSaveRestore.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

53.4.2 Bug Name 2

- Description:

  Sweep range should be per channel in JWL Cleanup step.

  In JWL Cleanup we calculate the maximum possible sweep range for the write cycle. This range depends on DQ/DQS delays of each byte, which were found in the previous step (JWL fine). MRC calculated a common sweep range for both channels.

  When we cannot find a passing cycle for a byte in one channel, we rerun the JWL cleanup with Dec_WRD = 0, to gain one more cycle to the sweep range.

  Now the sweep range may become incorrectly limited from the right side for the failing channel, because DQ/DQS values of the passing channel are already updated. Another minor issue is that Dec_WRD is changed for both channels, while it should be done per channel when needed.

- Solution

  Sweep range should be per channel. Dec_WRD should be changed only for the failing channel.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteLeveling.c

53.4.3 Bug Name 3

- Description:

  BIOS is not behaving as expected when mixing XMP and non-XMP DDR4 modules.

- Solution

  Added check in MrcCompareTimingProfiles to determine if DIMM is enabled, otherwise previous functionality in BIOS OC Setup Menu is broken.

  Changed XmpProfileEnable to be UINT8 for indicating which of the XMP profiles are enabled (0x3 if both are enabled)

Added check within SPD processing to determine identical timings for STD, XMP1, and XMP2. If the DIMMs do not have identical timing, XMP will not be enabled.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

  /KabylakePlatSamplePkg/Setup/OverClockSetup.hfr

  /KabylakeSiliconPkg/SystemAgent/Include/MemInfoHob.h

  /KabylakeSiliconPkg/SystemAgent/Include/Protocol/MemInfo.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

54 Version 1.0.4 Details

54.1 New Features

54.1.1 Feature 1

- Description / Solution

  Current MRC enables CKE Power Down when switching MC to Normal Mode, this includes SAGV frequency switch flow, where we go to Normal Mode in order to issue Self Refresh. Need to remove this Power Down enabling during SAGV switch, as it can cause issues with certain DRAMs.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

54.2 Fixed Bugs

54.2.1 Bug Name 1

- Description:

  During JEDEC Write Leveling Cleanup step, if DRAM doesn't toggle DQS on a read (can happen due to previous Write coming very early or very late), an old "good" data is passed from DDRIO to MC and being reported as PASS..

- Solution

  Increase the same rank WRWR turnarounds during JWL Cleanup, to avoid delayed data overlap with the expected data of the next write. This is an additional fix on top of what was done in KBL MRC 1.0.1.3.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/ WriteTraining/MrcWriteLeveling.c

55 Version 1.0.3 Details

55.1 New Features

55.1.1 Feature 1

- Description / Solution
  1. Added MrcGetMinimalEyeHeight() function.
  2. Update WriteVoltageCentering2D_DDR4() similar to DQTimeCentering1D():
     i. Program common center in Non-PDA fashion in order to make sure the PDA is successful.
     ii. Write using PDA only when we have a passing window.
  3. Bug fix in DQTimeCentering1D: non-PDA UpdateVrefWaitTilStable was called with UpdateHost = TRUE, hence was replacing per-byte MR6 values with the average value.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCommon.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.c

55.2 Fixed Bugs

55.2.1 Bug Name 1

- Description:

  KBL MRC: Updates to Retrain limits.

- Solution

  Print retrain limit values in MrcRetrainMarginCheck(). Increase WrV retrain limit from 160 to 170. Fix DDR4 WrV limits in MrcGetUpmPwrLimit().

- Platform Affected

All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

55.2.2 Bug Name 2

- Description:

  MrcGetCpuTime() is used with UINT32 variable, but it returns a UINT64 value. This can cause wrong timeout calculation in MRC.

- Solution

  Use UINT64 variable for MrcGetCpuTime() result.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcMemoryScrub.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Hal/MrcHalMiddleLevel.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcDdr3.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcIoControl.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcReset.c

55.2.3 Bug Name 3

- Description:

  During JEDEC Write Leveling Cleanup step, if DRAM doesn't toggle DQS on a read (can happen due to previous Write coming very early or very late), an old "good" data is passed from DDRIO to MC and being reported as PASS.

- Solution

  Flip the data pattern after each CPGC test in JWL Cleanup.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Source/WriteTraining/MrcWriteLeveling.c

55.2.4 Bug Name 4

- Description:

  Frequencies in OC Memory menu do not show real XMP values.

- Solution

  Show the real timings that the DIMM reports for XMP and not processed timings.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeFspBinPkg/Include/MemInfoHob.h

  KabylakePlatSamplePkg/Platform/PlatformSetup/Dxe/PlatformPolicySetup.c

  KabylakePlatSamplePkg/Setup/OverClockSetup.c

  KabylakeSiliconPkg/PolicyCheckInternalOnly/OffsetTable.txt

  KabylakeSiliconPkg/SystemAgent/Include/MemInfoHob.h

  KabylakeSiliconPkg/SystemAgent/Include/Protocol/MemInfo.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcSaveRestore.c

KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

56 Version 1.0.2 Details

56.1 New Features

N/A

56.2 Fixed Bugs

N/A

57 Version 1.0.1 Details

57.1 New Features

57.1.1 Feature 1

- Description / Solution

  Adjust Vtt panic comp threshold for more power savings : change VPANIC1 from 4 to 8

  .

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcMcConfiguration.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

57.2 Fixed Bugs

N/A

58 Version 1.0.0 Details

58.1 New Features

N/A

58.2 Fixed Bugs

N/A

59 Version 0.9.1 Details

59.1 New Features

N/A

59.2 Fixed Bugs

59.2.1 Bug Name 1

- Description:

  MMA test content has found false positive results due to inconsistencies between the register setting of TxVref and the assumed logical value of TxVref.

- Solution

  BiosSetMarginParamOffset will be changed to use UpdateVrefWaitTilStable directly.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Ssa/BiosSsaMemoryConfig.c

60 Version 0.9.0 Details

60.1 New Features

N/A

60.2 Fixed Bugs

N/A

61 Version 0.8.1 Details

61.1 New Features

61.1.1 Feature 1

- Description / Solution

  Added support for new Samsung DDR4 DDP parts which share the same CLK and ZQ pins across both ranks. Only CLK0 is used on CPU side, and it goes to both ranks in DDP package.

  Added two new input parameters to control this: Ddr4DdpSharedClock and Ddr4DdpSharedZq.

  MRC impact:

  - ShiftPIforCmdTraining(): when shifting CLK PI for rank 1, shift rank 0 as well (because Rank1 is connected to CLK0).

  - Set SCHED_CBIT.serialize_zq = 1 so that MC will serialize ZQ calibration due to shared ZQ pin.

  - During CMD normalization, only shift CLK0, otherwise ShiftPIforCmdTraining() will shift CLK0 twice.

  - Serialize ZQ calibration during JEDEC init.

  - Disable CLK1 buffer to save power.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/Include/ConfigBlock/MemoryConfig.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h
  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcSchedulerParameters.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcDdr3.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcMcConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

61.1.2 Feature 2

- Description / Solution

  Add Command Margin training steps: Slew Rate and Drive Strength / Equalization:

  - CMD Slew Rate training

  - CMD Drive Strength / Equalization training.

  This is needed in order to overcome low CmdT/CmdV margins at high speeds, especially on problematic boards. Both steps will only run on DDR4 in Margin Training cases (desktop).

  Additional changes:

  1. Separate Command Timing Normalization as a separate MRC task, because we need to do it only once after we finish LCT/CMDVC and the new CMD margin steps.
  2. Take out CMD timing centering from LCT as a separate function, because we need to re-center CMD timing during the new steps.
  3. Add Width support to "%s" format in MRC debug prints, it was only working with numbers.
  4. Use MRC_PRINTS_ON/OFF defines instead of TRUE/FALSE, for more readable code.
  5. Added MrcDisableCadbOnDeselect() to avoid code duplication in many places.
  6. Increase LCT loopcount from 10 to 14 according to EV feedback.
  7. Convert initial Slew Rate programming in MC Config to use the new UpdateSlewRateCompTargetValue() function.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakePlatSamplePkg/Include/SetupVariable.h

  /KabylakePlatSamplePkg/Library/PeiPolicyUpdateLib/PeiSaPolicyUpdatePreMem.c

  /KabylakePlatSamplePkg/Setup/SaSetup.hfr

  /KabylakePlatSamplePkg/Setup/SaSetup.uni

  /KabylakePlatSamplePkg/Setup/UqiList.uni

  /KabylakeSiliconPkg/SystemAgent/Include/ConfigBlock/MemoryConfig.h

  /KabylakeSiliconPkg/SystemAgent/Library/PeiSaPolicyLib/SaPrintPolicy.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcDebugHook.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcDebugPrint.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcDebugPrint.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCommandTraining.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCommon.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcCrosser.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcGlobal.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommon.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcMcConfiguration.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/WriteTraining/MrcWriteDqDqs.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c#9 edit Fixed Bugs

61.2 Fixed Bugs

61.2.1 Bug Name 1

- Description:

  CalcOptPowerByte calculates Tx slew rate incorrectly.

- Solution

  CalcOptPowerByte() reads CLK slew rate instead of DQ, and also does not convert from ScompCells to number of stages correctly..

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

62 Version 0.8.0 Details

62.1 New Features

N/A

62.2 Fixed Bugs

62.2.1 Bug Name 1

- Description:

  Skylake RC 1.7.0 has caused a regression in MRC CleanMemory handling: moving CleanMemory from MEMORY_CONFIGURATION into MEMORY_CONFIG_NO_CRC causes CleanMemory to not be honored on warm boots, causing a failure to honor TCG MOR Request.

- Solution

  Fixed missing logic to properly comunicate to ME FW that memory has been scrubbed.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

62.2.2 Bug Name 2

- Description:

  Skylake RC 1.7.0 has caused a regression in MRC CleanMemory handling: moving CleanMemory from MEMORY_CONFIGURATION into MEMORY_CONFIG_NO_CRC causes CleanMemory to not be honored on warm boots, causing a failure to honor TCG MOR Request.

- Solution

  Fixed missing logic to properly comunicate to ME FW that memory has been scrubbed.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

62.2.3 Bug Name 3

- Description:

  MRC 0.6.0.6 enabled full grid sweep in DIMM ODT training for DDR4 1DPC. This should be done for Margin training case only, not for Power training.Power training mode enables sub-optimizations, and full grid takes too much time.

- Solution

  Full grid DIMM ODT in 1DPC should be enabled for margin training, not for power training.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

62.2.4 Bug Name 4

- Description:

  System hangs during Capsule update.

- Solution

  System hangs during Capsule update.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

62.2.5 Bug Name 5

- Description:

  Should swap the order of Roundtrip Latency and Turnaround optimization steps with the 2D steps. The TAT/RTL should come before the 2D steps.

- Solution

  Swap the order of TAT/RTL steps and 2D steps

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcInterpreter.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

63 Version 0.7.3 Details

63.1 New Features

63.1.1 Feature 1

- Description / Solution

  StubMrc fixes / improvements:

  1. Skip DllBwEn reset for both STUB and LOCAL_STUB
  2. Add VccIomV to INI file
  3. Both Stub client and StubServer should use static libraries instead of DLL for Runtime library.
  4. Initialize DMIBAR before calling MRC core.
  5. StubServer: try both Debug and Release versions of IUnmanaged.dll, because sometimes one of them fails.
  6. StubServer: test MCHBAR and PCI register access at startup, to flag ITP issues to the user.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcStartMemoryConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/MrcVisualStudio/VS2012/StubMrc/Stub.vcxproj

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/MrcVisualStudio/VS2012/StubMrc/StubMrc.ini

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/MrcVisualStudio/VS2012/StubServer/StubServer.vcxproj

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/StubCode/Client/Stub.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/StubCode/Server/StubServer.cpp

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/StubCode/StubModeProtocol.h

63.2 Fixed Bugs

63.2.1 Bug Name 1

- Description:

  MrcSetupVtt uses hard-coded value of 162 Ohms for CMD Target. This causes higher power consumption with DDR3/DDR4 in Vtt mode.

- Solution

  Fix the formula to use the actual CMD Ron target.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcMcConfiguration.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcMcConfiguration.c

63.2.2 Bug Name 2

- Description:

  Restore S3 resume MTRRs before giving control to OS.

- Solution

  Restore S3 resume MTRRs before giving control to OS.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakePlatSamplePkg/FspWrapper/Library/PeiFspPolicyInitLib/PeiFspCpuPolicyInitLib.c

  /KabylakePlatSamplePkg/FspWrapper/Library/PeiFspPolicyInitLib/PeiFspPolicyInitLib.inf

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

63.2.3 Bug Name 3

- Description:

  MRC is currently setting DDR4 Self Refresh to 'Normal Operating Temperature Range), meaning, it is being set to b00. MRC shall be setting DDR4 Self Refresh to 'ASR Mode (Auto Self Refresh)', meaning, set the bits to b11.

- Solution

  Modified code to ensure DDR4 Self Refresh feature is set to 'ASR Mode'.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/DimmCellTest/MrcDimmCellTest.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcMemoryMap.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcDdr3.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Common/PlatformBoardId.h

64 Version 0.7.2 Details

64.1 New Features

64.1.1 Feature 1

- Description / Solution

  Basin Falls memory POR frequencies for KBL-X CPU are :

  1600/1866/2133/2400/2666 (1DPC)

  1600/1866/2133/2400 (2DPC)

  Stretch: DDR4-3200 (1DPC)

  Need MRC to add the option for 2666 speed as POR.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcPowerModes.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcTimingConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcDdr3.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcMcConfiguration.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

64.2 Fixed Bugs

64.2.1 Bug Name 1

- Description:

  KBL-PO-H0 RVP15 and rvp5 are booting to 1600 instead 2133 fused with QKUF.

- Solution

  Need to remove the old CPUID check for SKL A0/B0/P0 which didn't have CAPID0_C implemented.

  Also print the decoded value of DMFC for easy debug.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

64.2.2 Bug Name 2

- Description:

  KBL-DT: Board ID is shown as 'TBD' in BIOS setup on KBL-S board.

- Solution

  Updated the KBL S board ID SKU's accordingly.

- Platform Affected

  KBL-S board

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Common/PlatformBoardId.h

64.2.3 Bug Name 3

- Description:

  Current MRC programs RefPi to 7 regardless if it's SKL or KBL.

- Solution

Need to program it to 7 only on KBL, and keep default value (0) on SKL.

- Platform Affected

  All Kaby Lake Platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcMcConfiguration.c

65 Version 0.7.1 Details

65.1 New Features

65.1.1 Feature 1

- Description / Solution

  KBL OC: Choosing XMP profile as memory profile will set the memory speed at highest even ratio and not at the highest odd ratio

  Added an option to automatically select Odd Ratio Mode in Default/XMP1/XMP2 profiles, if it gives us a DDR frequency closer to the actual DRAM tCK.

  In Custom profile the Inputs->OddRatioMode will be used as is, without override.

  Save OddRatioMode in MrcSaveData struct for Warm/Fast flows.

  Minor fixes for local stub mode.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcSaveRestore.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/StubCode/Client/LocalStub.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/StubCode/Client/Stub.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/StubCode/Client/Stub.h

65.2 Fixed Bugs

65.2.1 Bug Name 1

- Description:

  PRMRR Memory region needs to be programmed as WRITE_BACK in the MTRR.

- Solution

  Added in MRC Memory Map a type of memory to help identify the memory regions that need to be RESERVED and have WRITE_BACK capability and modified Platform code in charge of setting MTRR to check for this extra memory type to ensure it is part of the MTRR

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MemoryInit.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

65.2.2 Bug Name 2

- Description:

  Merge from SKL MRC: W/A for MC may lose RCH completion credits while it enables clock gating.

- Solution

  MRC need to set the following bits to disable clock gating:

  MCDECS_CR_MC_GLOBAL_DRIVER_GATE_CFG.MNT_GLB_DRV_GATE_DIS = 1

  MCDECS_CR_MC_GLOBAL_DRIVER_GATE_CFG.MAINS_GLB_DRV_GATE_DIS = 1

- Platform Affected

  All KabyLake platforms

- Affected Files:

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

/KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcSchedulerParameters.c

65.2.3 Bug Name 3

- Description:

  Merge from SKL MRC: Initial RecvEn PI setting is not optimal for DDR4 1867 in some cases.

- Solution

  Need to start Read Leveling from PI = 0 instead of 128 for 1867 and up, to avoid PI overflow in Step 4/5.

  The code was checking FreqMax instead of current Frequency, and also it was checking for above 1867 and not including 1867.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/ReadTraining/MrcReadReceiveEnable.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/Prep.bat

65.2.4 Bug Name 4

- Description:

  MRC MEMORY_CONFIG_NO_CRC.CleanMemory is not honored on warm reset

  Skylake RC 1.7.0 has caused a regression in MRC CleanMemory handling:

  - Revision 13:

  - For 1.7.0 releases\n

  - Deprecated MEMORY_CONFIGURATION -> CleanMemory\n

  - Added MEMORY_CONFIG_NO_CRC -> CleanMemory\n

  We have found that moving CleanMemory from MEMORY_CONFIGURATION into MEMORY_CONFIG_NO_CRC causes CleanMemory to not be honored on warm boots, causing a failure to honor TCG MOR Request.

- Solution

  Force MRC Fast Boot flow to ensure memory scrubbing is executed during Warm Boot if TCG MOR request is set.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  /KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

66 Version 0.7.0 Details

66.1 New Features

66.1.1 Feature 1

- Description / Solution

  Modified required files to ensure MRC uses the GetRandomNumber32 function from MdePkg. Updated MiniBIOS function to match the one from MdePkg and be compatible with new definition

  Move Rng Library to ClientSiliconPkg\SampleCode, Replace calls to RNG library to the clientSiliconPkg instance (Currently BiosGuard and MRC are the consumers of this lib), Remove client CPU RC copy of RNG library (BaseCpuRngLib)

  Any silicon specific overrides needs to be maintained within CPU reference code.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  Variose files under KabylakeSiliconPkg.

66.1.2 Feature 2

- Description / Solution

  Break the current HOB_SAVE_MEMORY_DATA which includes everything MRC is outputting (Inputs, Outputs, Save, etc) into 2 separate HOBs. One HOB that only has the Save info (MrcSave). Second HOB that has the rest.

  Generated 3 different HOBs:

  1st has MrcSava

  2nd has SMBIOS and OC data

  3rd has platform miscellaneous information

- Platform Affected

  All KabyLake platforms

- Affected Files:

  Variose files under KabylakeFspBinPkg, KabylakeFspPkg, KabylakeSiliconPkg.

66.1.3 Feature 3

- Description / Solution

  Add full grid sweep in DIMM ODT training for DDR4 1DPC - adds about 35% TxV margin for 2400 MT/s.

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

66.2 Fixed Bugs

66.2.1 Bug Name 1

- Description:

  Skylake RC 1.7.0 has caused a regression in MRC CleanMemory handling. Moving CleanMemory from MEMORY_CONFIGURATION into MEMORY_CONFIG_NO_CRC causes CleanMemory to not be honored on warm boots, causing a failure to honor TCG MOR Request.

- Solution

  Force MRC Fast Boot flow to ensure memory scrubbing is executed during Warm Boot if TCG MOR request is set

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/MemoryInit.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

66.2.2 Bug Name 2

- Description:

  Bios SSA Variable and Results GUIDs missing in EvLoader code.

- Solution

  Add missing GUIDs back into EvLoader code by correctly defining in SiPkg.dec

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiEvLoaderLib/EvLoaderPeim.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiEvLoaderLib/EvLoaderPeim.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiEvLoaderLib/PeiEvLoaderLib.inf

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

66.2.3 Bug Name 3

- Description:

  Bug fix in CalcOptPowerByte() for write power calculation.

- Solution

  Write ODT was passed instead of Non-target write ODT into MrcGetEffDimmWriteOdt().

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

66.2.4 Bug Name 4

- Description:

  Bug fix in CalcOptPowerByte() for write power calculation.

- Solution

  Write ODT was passed instead of Non-target write ODT into MrcGetEffDimmWriteOdt().

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

66.2.5 Bug Name 5

- Description:

  Fix CompOptimization corner case with COMP code down.

- Solution

  Fix CompOptimization corner case with COMP code down

- Platform Affected

  All KabyLake platforms

- Affected Files:
- KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h
- KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCrosser.c

67 Version 0.6.1 Details

67.1 New Features

N/A

67.2 Fixed Bugs

67.2.1 Bug Name 1

- Description:

  Selected Memory timing override values are not displayed correctly. When loading XMP profile or reverting to default values, the timing values are not updated on the screen. They only show up properly after a reboot. We require this mechanism to work on the fly so we can manually modify timings derived from XMP profiles.

- Solution

  Added functionality to OC Setup Menu to dynamically update based on chosen Memory Profile.

  tCK values in OC Setup Menu are now displayed in MHz instead of femtoseconds

  Added Memory Ratio = 3 option to OC Setup Menu

- Platform Affected

  All KabyLake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Include/MrcInterface.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.h

68 Version 0.6.0 Details

68.1 New Features

68.1.1 Feature 1

- Description / Solution

  Splitting FspUpdVpd.h to FsptUpd.h/FspmUpd.h/FspsUpd.h

- Platform Affected

FPS Only

- Affected Files:

  Variose files under KabylakeFspBinPkg.

68.1.2 Feature 2

- Description / Solution

  MRC returns an error when RDIMMs and/or mixed UDIMM/RDIMM are detected on a platform.

  MRC will halt if RDIMM is present on the system. Force MRC to halt and fail if Non ECC DIMM is detected on the system when FDEE bit is set.

- Platform Affected

  All Skylake /Kaby Lake platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcInterpreter.c

- KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h
- KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/SpdProcessing/MrcSpdProcessing.c
- KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c
- KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/StubCode/Client/LocalStub.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Restricted/StubCode/Client/Stub.c

68.2 Fixed Bugs

68.2.1 Bug Name 1

- Description:

  New KBL RVP3 boards have Rtt resistors removed on CMD/CTL/CLK. LPDDR3 Early Command Training fails sometimes on these boards at 1867, and passes at 1600

- Solution

  The first step of ECT (2D CS/CMD search) was getting a working CMD value but marginal CS value. Fix the 2D CS/CMD search to find 3 passing points of CS after a good CMD point was found, thus ensuring good margin on both sides for both CMD and CS. Remove memory frequency limit to 1600 for KBL RVP3 board.

  Also add KBL RVP3 support to MRC MiniBios.

- Platform Affected

  KabyLake RVP3 LPDDR3 based platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Services/MrcCommandTraining.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

68.2.2 Bug Name 2

- Description:

  CAT Error during PCI scan on MiniBios

- Solution

  Disable PCIe root ports on PCH at the beginning of MiniBios, to avoid a hang / CATERR during PCI scan in ITP.

- Platform Affected

  MiniBios Only

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

68.2.3 Bug Name 3

- Description:

  Margin overflow in GetPdaMargins. INT8 variable is used to hold a margin offset in GetPdaMargins() routine, and when this offset is greater than 12 ticks it overflows INT8 variable due to multiplication by a factor of 10.

  This causes wrong WrV margins calculation and memory failures.

- Solution

  Use INT16 instead of INT8 for MarginOffset variable..

- Platform Affected

  All DDR4 platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcOemPlatform.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/MiniBios/MEMORY/MrcSetup.c

68.2.4 Bug Name 4

- Description:

  Need mcdecs_misc_0_0_0_mchbar_mcmain.spare_rw[4:0] = 0b10000 to periodically override the external VC1Demote signal to 0 for a short window and turn high priority for 64 cycles every 1024 cycles.Margin overflow in GetPdaMargins.

- Solution

  Implement the operation as described above.

- Platform Affected

  All platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/McConfiguration/MrcSchedulerParameters.c

68.2.5 Bug Name 5

- Description:

Setting SAGV fixed to LOW does not change FCLK frequency. It only changes QCLK frequency.

- Solution

  Added required logic to communicate with the CPU PCODE through MAILBOX and send proper command and value to execute the requested change when SAGV is set to FixedLow.

- Platform Affected

  All platforms

- Affected Files:

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcApi.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.c

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Api/MrcGeneral.h

  KabylakeSiliconPkg/SystemAgent/MemoryInit/Library/Private/PeiMemoryInitLib/Source/Include/MrcVersion.h

68.3 Unsupported Features

N/A

68.4 Known Issues

N/A

69 Version 0.5.0 Details

Initial Release

69.1 New Features

None

69.2 Fixed Bugs

None

69.3 Known Issues

None

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